WHAT IS CLAIMED IS:

1. A method for controlling a digital phase lock loop (DPPL), the method comprising the steps of:

providing a DPLL having a digital controlled oscillator (DCO);

storing the present active state of the DPLL; and

removing primary power to the DPLL subsequent to storing its present active state.

2. The method according to claim 1, wherein the step of storing the present active state of the DPLL comprises placing selective DPLL digital elements having register retention capability into a low power standby mode.

3. The method according to claim 1, further comprising the steps of:

reasserting the primary power to the DPLL; and

restoring the present active state of the DPLL.

4. The method according to claim 3, wherein the step of restoring the present active state of the DPLL comprises the steps of:

aligning a DCO feedback clock with a reference clock; and

simultaneously with aligning the DCO feedback clock with a reference clock, controlling the DCO such that its output clock frequency is substantially identical with its frequency prior to removal of the primary DPLL power.

5. The method according to claim 4, wherein the step of controlling the DCO such that its output clock frequency is substantially identical with its frequency prior to removal of the primary DPLL power, comprises the steps of:

rolling back a DCO control code such that the DCO restarts at a slightly lower clock frequency than the frequency at which the DCO most previously was locked; and

detecting if and when a targeted DCO output clock frequency has been achieved.

6. The method according to claim 5, wherein the step of detecting if and when a targeted DCO output clock frequency has been achieved comprises the step of detecting a normalized frequency lock to determine whether the targeted DCO output clock frequency is locked within a desired percentage of a desired DCO output clock frequency.

7. A digital phase lock loop (DPLL) comprising:

a digital controlled oscillator (DCO);

a digital controller operational to generate DCO control codes;

a reference clock;

a phase frequency detector (PFD);

a time digitizer operational to convert phase error between reference and feedback clocks into a digital control code such that the digital controller is controlled there from;

a feedback loop from the DCO output to generate the feedback clock to the PFD input; and

algorithmic control software, wherein the DPLL operates in response to the algorithmic control software to store the present active state of the DPLL and remove primary power to the DPLL subsequent to storing its present active state.

8. The DPLL according to claim 7, wherein the DPLL further operates in response to the algorithmic control software to reassert the primary power to the DPLL and restore the present active state of the DPLL.

9. The DPLL according to claim 7, wherein the DPLL further operates in response to the algorithmic control software to reassert the primary power to the DPLL, align the DCO output clock with the reference clock and simultaneously control the DCO such that its output clock frequency is substantially identical with its frequency prior to removal of the primary DPLL power.

10. The DPLL according to claim 7, wherein the DPLL further operates in response to the algorithmic control software to reassert the primary power to the DPLL, align the DCO output clock with the reference clock and simultaneously roll back the DCO control code such that the DCO restarts at a slightly lower clock frequency than the frequency at which the DCO most previously was locked and detect if and when a targeted DCO output clock frequency has been achieved.

11. The DPLL according to claim 7, wherein the DPLL further operates in response to the algorithmic control software to reassert the primary power to the DPLL, align the DCO output clock with the reference clock and simultaneously roll back the DCO control code such that the DCO restarts at a slightly lower clock frequency than the frequency at which the DCO most previously was locked and detect a normalized frequency lock to determine whether the targeted DCO output clock frequency is locked within a desired percentage of a desired DCO output clock frequency.